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Near-Optimal Performance with a Significant Reduction in the Complexity for MIMO SC-FDMA Systems

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ABSTRACT*:* Large-scale multiple-input multiple output is termed to be one of the key technology in future generation multiple cellular systems supporting the 3GPP LTE. LTE includes MIMO technology with orthogonal frequency division-multiple access technology surrounded by the downlink and single carrier-frequency division multiple access (SC-FDMA). This paper introduces a novel low-complexity multiple-input multiple-output (MIMO) detector tailored for single-carrier frequency division-multiple access (SC-FDMA) systems, suitable for efficient hardware implementations. The proposed detector starts with an initial estimate of the transmitted signal based on a minimum mean square error (MMSE) detector. Subsequently, it recognizes less reliable symbols for which more candidates in the constellation are browsed to improve the initial estimate. An efficient high-throughput VLSI architecture is also introduced achieving a superior performance compared to the conventional MMSE detectors. The performance of the proposed design is close to the existing maximum likelihood post-detection processing (ML-PDP) scheme, while resulting in a significantly lower complexity, i.e., and times fewer Euclidean distance (ED) calculations in the 16-QAM and 64-QAM schemes, respectively.

KEYWORDS: ASIC implementation, LTE, MIMO, PDP, SC-FDMA, soft decoding.

I. INTRODUCTION

Very large scale integration (VLSI) is the process of creating an integrated circuit (IC) by combining thousands of transistors into a single chip. The microprocessor is a VLSI device. Before the introduction of VLSI technology most ICs had a limited set of functions they could perform. An electronic circuit might consist of a CPU, ROM, RAM and other glue logic. VLSI lets IC designers add all of these into one chip. The first semiconductor chips held two transistors each. Subsequent advances added more transistors, and as a consequence, more individual functions or systems were integrated over time. The first integrated circuits held as ten diodes, transistors, resistors and capacitors, making it possible to fabricate one or more logic gates on a single device known retrospectively as small-scale integration(SSI), improvements in technique led to devices with hundreds of logic gates, known as medium-scale integration (MSI). Further improvements led to large-scale integration (LSI), i.e. systems with at least a thousand logic gates. Multiple-input multiple-output (MIMO) along with spatial multiplexing develops the basic of most modern wireless communication standards, such as 3GPP LTE or IEEE 802.11n . MIMO technology avails considerably higher data rates over single-antenna systems by transmitting multiple data streams at the same time as and in the same frequency band. Conventional MIMO wireless systems, though, already start to approach their throughput limits. Consequently, the consumption of new transceiver technologies is of supreme importance in order to meet the ever-growing demand for higher data rates, better link reliability, and improved coverage, without further increasing the communication bandwidth. The 3rd generation partnership project considered to meet the needs of the 4G wireless communication. LTE along with the multiple-input multiple-output system with frequency OFDMA technology in the downlink and single carrier-frequency division multiple access (SC-FDMA) in the uplink to accomplish peak data rates of 350 Mbps and 80 Mbps, respectively. LTE-Advanced (LTE- A), which is a progress of

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LTE, supports single-user spatial multiplexing of up to eight layers in the downlink and four layers in the uplink targeted to achieve peak data rates of 1 Gbps and 500 Mbps, respectively. The SC-FDMA utilizes a discrete Fourier transform-spread OFDM (DFT-S-OFDM) modulation with similar performance compared to the OFDM. Its main advantage is to provide a lower peak-to-average power ratio (PAPR), which makes it the technology of the choice for the uplink. However, the implementation of a MIMO detector in an SC-FDMA system is significantly more complicated than that of an OFDMA system. This occurs because that sent information is added due to the extra DFT block employed naturally in an SC-FDMA technique. Therefore, the implementation of a low-complexity MIMO detector is needed and is the main challenge in the SC-FDMA framework. Several have been proposed for SC-FDMA MIMO detectors among which the linear frequency domain equalizer (FDE) receivers, including the minimum mean square error (MMSE) and zero forcing (ZF), are often used due to their simplicity. Similar to the case of MIMO systems, successive interference cancellation and iterative techniques can be used to enhance the performance of receivers. However, these techniques introduce long delays due to their iterative nature. The maximum likelihood (ML) receiver also, offers an optimal bit error rate (BER) performance but incurs very high computational complexity particularly in the SC-FDMA receivers. Taking into account the negotiation between the BER performance and the complexity, normally suboptimal methods are engaged. In this paper, a recognition method is suggested for MIMO SC-FDMA systems, which provides near-optimal performance with an important decrease in the complication particularly for huge constellation sizes.

II. RELATED WORK

A FAST RECURSIVE ALGORITHM FOR OPTIMUM SEQUENTIAL SIGNAL DETECTION IN A BLAST SYSTEM
Jacob Benesty,Yiteng Arden Huang and Jingdong Chen (July 2003)

Bell Laboratories layered space-time (BLAST) wireless systems are multiple-antenna communication schemes that can achieve very high spectral efficiencies in scattering environments with no increase in bandwidth or transmitted power. The most popular and, by far, the most practical architecture is the so-called vertical BLAST (V-BLAST). The signal detection algorithm of a V-BLAST system is computationally very intensive. If the number of transmitters is M and is equal to the number of receivers, this complexity is proportional to 4 at each sample time. In this paper, we propose a very simple and efficient algorithm that reduces the complexity by a factor of M

ASIC IMPLEMENTATION OF SOFT-INPUT SOFT-OUTPUT MIMO DETECTION USING MMSE PARALLEL INTERFERENCE CANCELLATION
ChristophStuder,SchekebFateh and Dominik Seethaler (July 2011)

Multiple-input multiple-output (MIMO) technology is the key to meet the demands for data rate and link reliability of modern wireless communication systems, such as IEEE 802.11nor 3GPP-LTE. The full potential of MIMO systems can, however, only be achieved by means iterative MIMO decoding relying on soft-input soft-output (SISO) data detection. This paper describes the first ASIC implementation of a SISO detector for iterative MIMO decoding. To this end, we propose a low-complexity minimum mean-squared error (MMSE) based parallel interference cancellation algorithm, develop a suitable VLSI architecture ,and present a corresponding four-stream 1.5 mm detector chip in90 nm CMOS technology. The fabricated ASIC includes all necessary pre-processing circuitry and exceeds the 600 Mb/s peak data rate of IEEE 802.11n. A comparison with state-of-the-art MIMO detector implementations demonstrates the performance benefits of our ASIC prototype in practical system-scenarios.

A LOW-COMPLEXITY HIGH-THROUGHPUT ASIC FOR THE SC-FDMA MIMO DETECTORS
K. Neshatpour, M. Mahdavi, and M. Shabany (May 2012)

A novel low-complexity detection scheme is proposed for the multiple-input multiple-output (MIMO) single-carrier frequency division-multiple access (SC-FDMA) systems, which is suitable for ASIC implementations. The proposed detection scheme makes an initial estimate of the transmitted signal based on a minimum mean square error (MMSE) frequency domain equalizer (FDE) detector and finds symbols with higher error probability among them and browse more candidates for them in the constellation to improve their initial estimate. Based on this approach, architecture is introduced that achieves superior bit error rate (BER) performance compared to the conventional MMSE FDE.

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The performance of the proposed design is close to the existing maximum likelihood-post detection processing (ML-PDP) scheme, while achieving a significantly lower complexity, i.e., 450× less Euclidean distance (ED) calculations in 16-QAM. The ASIC implementation of the proposed architecture, the first ASIC for SC-FDMA detectors to-date, achieves a 3× higher throughput than the best design reported to-date.

III. EXISTING SYSTEM

The 3rd generation partnership project (3GPP) defined long term evolution (LTE) to meet the requirements of the 4G wireless communication. LTE combines multiple-input multiple-output (MIMO) technology with orthogonal frequency division-multiple access (OFDMA) technology in the downlink and single carrier-frequency division multiple access (SC-FDMA) in the uplink to achieve peak data rates of 300 Mbps and 75 Mbps, respectively. LTE-Advanced (LTE-A),which is an evolution of LTE, supports single-user spatial multiplexing of up to eight layers in the downlink and four layers in the uplink targeted to achieve peak data rates of 1 Gbps and 500 Mbps, respectively.

The SC-FDMA utilizes a discrete Fourier transform-spread OFDM (DFT-S-OFDM) modulation with similar performance compared to the OFDM. Its main advantage is to provide a lower peak-to-average power ratio (PAPR), which makes it the technology of the choice for the uplink. However, the implementation of a MIMO detector in an SC-FDMA system is significantly more complicated than that of an OFDMA system. This is due to the fact that the transmitted data is mixed together because of the extra DFT block used naturally in an SC-FDMA system. Therefore, the implementation of a low-complexity MIMO detector is needed and is the main challenge in the SC-FDMA framework

IV. PROPOSED METHOD

In this paper, a detection scheme is proposed for MIMO SC-FDMA systems, which provides near-optimal performance with a significant reduction in the complexity especially for large constellation sizes. The proposed design is fabricated in a 0.13 CMOS technology and fully tested. Moreover, in order to benefit from the enhanced signal integrity offered by coded systems, the proposed hard decoding architecture is also modified to create optimized for area and the other, optimized for a better BER performance.

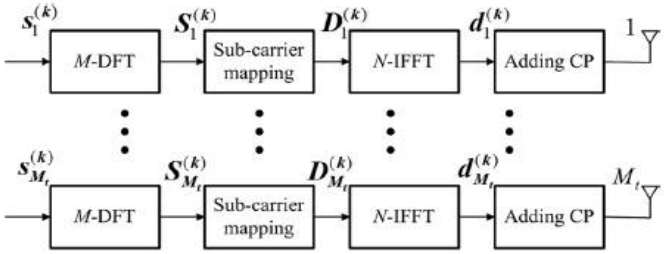

Fig. 1. MIMO SC-FDMA transmitter for user k with M_t transmit antennae.

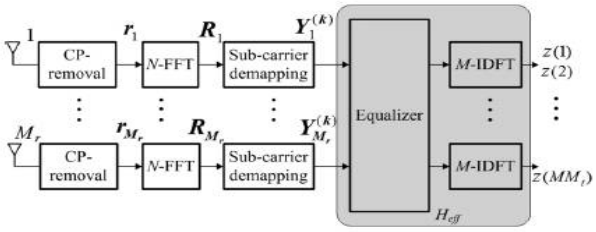

Fig. 2. MIMO SC-FDMA receiver for user k with M_r receive antennae.

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MIMO SC-FDMA MODEL

The MIMO single carrier FDMA design model has a transmitter and receiver which are discussed as follows.

A. TRANSMITTER

The transmitter side of a MIMO SC-FDMA system with Mt transmit and Mr receive antennae supporting K users as shown in figure 1.

The data stream on each transmit antenna is grouped into blocks of M symbols, as follows,

$$\boldsymbol{s}_{\boldsymbol{n_t}}^{(\boldsymbol{k})} = \left[s_{n_t}^{(k)}(0), s_{n_t}^{(k)}(1), \ldots, s_{n_t}^{(k)}(M-1) \right]^T$$

where the superscriptT represents the transpose operation,

n_t is the antenna index, M is the DFT size, and $\mathbf{S^{(k)}n_t}$ represents the data on the transmit antenna n_t for user k, whose elements are chosen from Q-aray quadrature amplitude modulation (QAM) constellation. After the DFT operation, the frequency domain (FD) representation of data on antenna n_t is obtained and is denoted by $\mathbf{S^{(k)}n_t}$

B. RECEIVER

A conventional linear SC-FDMA detector for user K is depicted in Fig. 2. After the CP removal on antenna n_t at the SC-FDMA receiver with Mr receive antennae, the received signal is denoted as

$$\boldsymbol{r}_{\boldsymbol{n_r}} = \sum_{k=1}^{K} \sum_{n_t=1}^{M_t} h_{n_r,n_t}^{(k)} \otimes_N \boldsymbol{D}_{\boldsymbol{n_t}}^{(\boldsymbol{k})} + \boldsymbol{w}_{\boldsymbol{n_r}}$$

The proposed system shown in figure 3 uses LBC (Linear Block Code) to detect and correct the error. Errors corrected in the message block. Encoded using more symbols with accurate original value. The LBC are used in forward error correction and applied in transmitting symbols on a communication channel. The dashed lines in the architecture denote a number of the pipelining stages. The inputs of the architecture are the channel coefficients, the outputs of the MMSE detector, and the received FD signals at the receiver. In fact, the "H" inputs represent the values of all the terms in the t-th row in Heff at the t-th clock cycle, the

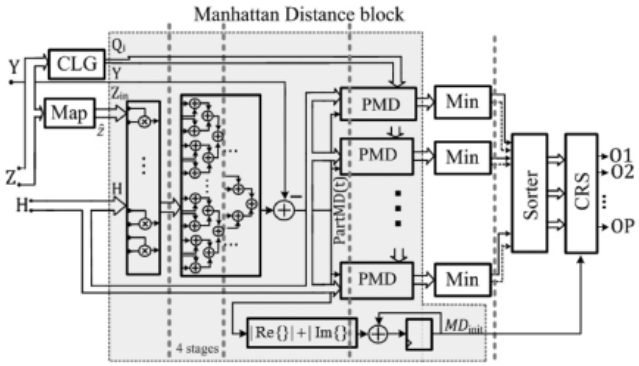

Figure 3 Proposed architecture

"Z" inputs are the outputs of the first stage, and the "Y" input represents the t-th element in Y at the t-th clock cycle.

The architecture performs the detection in clock cycles.

The Min blocks in Fig. 3 calculate the lowest values of the MDs derived by the PMD blocks for each symbol along with their corresponding constellation points. Since P clock cycles are required to produce the EP metric values, the sorting can also be done in P clock cycles using a minimum hardware, which results in the minimum values of EP metrics and their corresponding constellation points along with indices indicating the symbols selected as the erroneous symbols.

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V. SIMULATION RESULTS

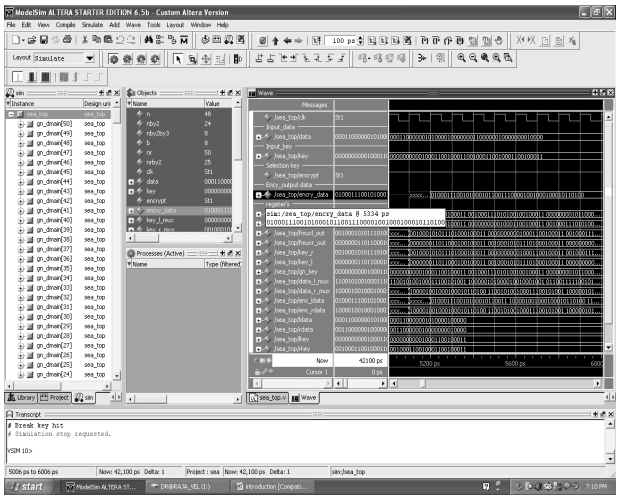

Fig 4: Scalable Encryption

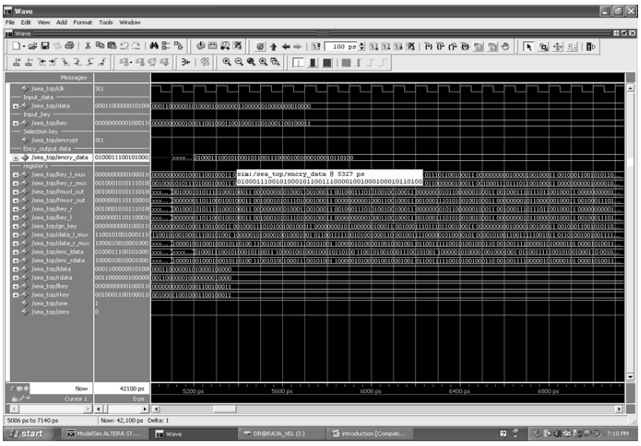

Fig 5: Scalable Encryption Binary Format

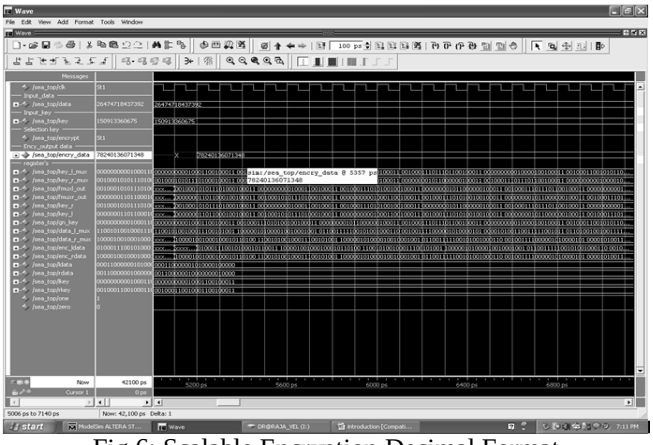

Fig 6: Scalable Encryption Decimal Format

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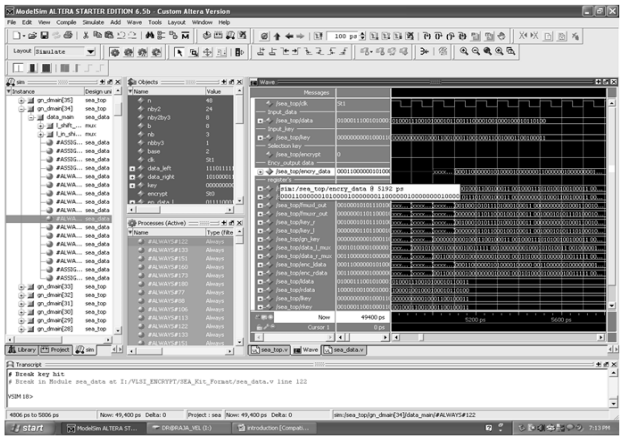

Fig 7: Scalable Decryption

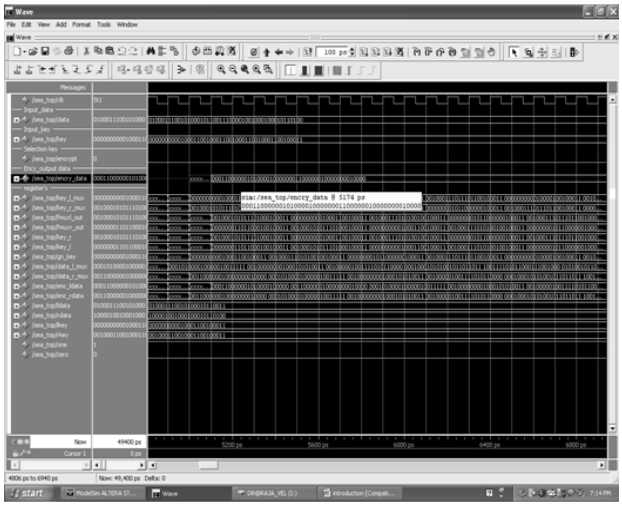

Fig 8: Scalable Decryption Binary Format

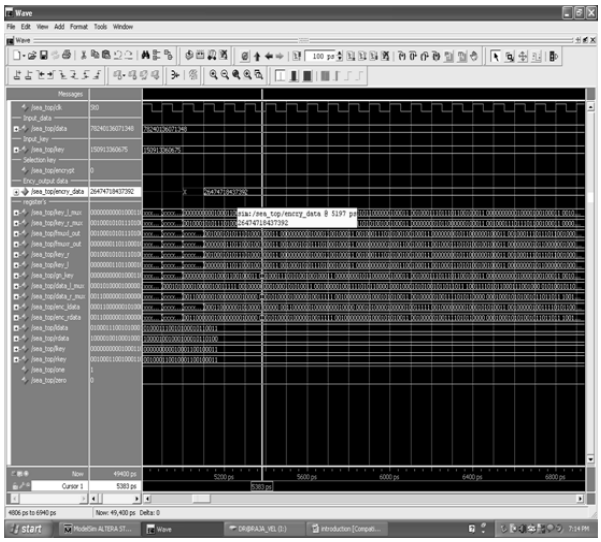

Fig 9: Scalable Decryption Decimal Format

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VI. CONCLUSION

The BER performance of the proposed detection scheme is close to ML-PDP while the reduction in the complexity is significant in large constellation sizes. A soft decoding MIMO detector with reasonable complexity was also implemented for a MIMO SC-FDMA coded system, resulting in significant enhancement in the performance. In future, the BER (Bit error Ratio) performance of the proposed detection scheme is close to Previous Methods that has been implemented while the reduction in the complexity is significant in large constellation sizes. A soft decoding MIMO detector with reasonable complexity was also implemented for a MIMO SC-FDMA coded system, resulting in significant enhancement in the performance. By using both the Soft and Hard Decoding methods the given sample BER (Bit error Ratio) could be comparatively reduced and so the complexity of the system.

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